480μA , 6 .5MHz , RR IO C MOS Operational amplifier

Overview

The SL8631 (single), SL8632 (dual), and SL8634 (quad) are low-noise, low-voltage, and micropower operational amplifiers. The SL863x family features 6.5MHz bandwidth, 4V/μs slew rate, and 480μA quiescent current per amplifier (5V supply voltage). The SL863x family of operational amplifiers can be designed into a wide range of applications.

The SL863x operational amplifiers are designed to provide optimal performance for low-voltage and low-noise systems. Their input common-mode voltage range includes ground, and the maximum input offset voltage is 4.2mV. The SL863x can provide rail-to-rail output swing under heavy output loads. The SL863x family is suitable for single or dual supplies from +2.1V to +5.5V. All models are specified to operate over the extended industrial temperature range of -40℃ to +125℃.

The SL8631 is available in 5-pin SC70 and SOT-23 packages. The SL8632 is available in 8-pin MSOP, DFN2*2, TSSOP, and SOP packages. The SL8634 is available in 14-pin TSSOP and SOP packages.

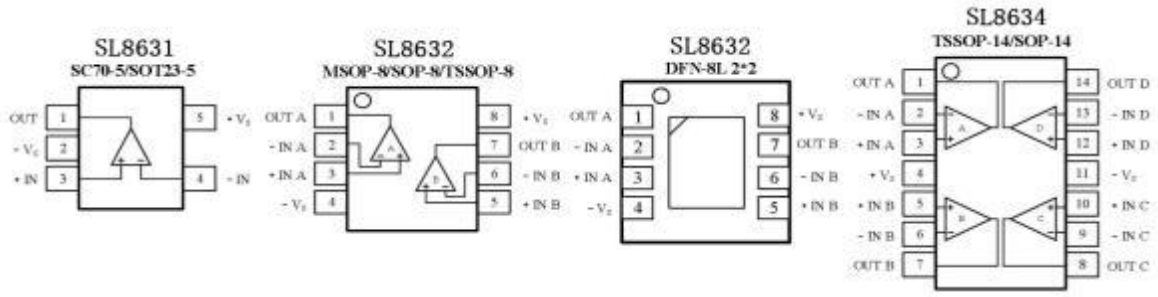
Features

- High conversion rate: 4V/μs
- Gain bandwidth product: 6.5MHz
- Low power: 480μA supply current per amplifier
- Settling time to 0.1% (2V step): 1μs
- Low noise: 20nV/√Hz@10kHz
- High gain: 103dB
- Low offset voltage: 4.2mV (maximum)
- Unity-gain stable
- Rail-to-rail input and output
  - Input voltage range: -0.1V to +5.1V (5V supply voltage)
- Operating supply range: +2.1V to +5.5V
- Operating temperature range: -40°C to +125°C

Application

- Photodiode and sensor interface
- Audio output
- Active filter
- Driving A/D converters
- Portable and battery-powered devices

Pin distribution



Picture 1. Pin distribution

Pin description

Symbol	Description
-IN	Negative (inverting) input terminal.
+IN	Positive (non-inverting) input terminal.
-INA, -INB -INC, -IND	At the inverting input of the amplifier, the voltage can range from (VS– – 0.1V) to (VS+ + 0.1V).
+INA,+INB +INC, +IND	The noninverting input of the amplifier, this pin has the same voltage range as –IN.
+VS	Positive supply terminal, voltage is 2.1V to 5.5V. A 0.1μF bypass capacitor should be used between the supply pins or between the supply pins and ground as close to the device as possible.
-VS	Negative supply terminal, usually connected to ground. It can also be connected to a voltage other than ground as long as the voltage between VS+ and VS– is between 2.1V and 5.5V. If it is not connected to ground, bypass it with a 0.1μF capacitor as close to the part as possible.
OUTA, OUTB OUTC, OUTD	Amplifier output.
OUT	Output end.

Ordering information

Model	Package	Boxing quantity
SL8631XC5	SC70-5	3000roll plate
SL8631XT5	SOT23-5	3000roll plate
SL8632XS8	SOP-8	3000roll plate
SL8632XV8	MSOP-8	3000roll plate
SL8632XF8	DFN-8	3000roll plate
SL8632XT8	TSSOP-8	3000roll plate
SL8634XT14	TSSOP-14	3000roll plate
SL8634XS14	SOP-14	2500roll plate

Absolute maximum ratings (TA=25℃)

Symbol	Description	Rating	Unit
$V_{S+,}V_{S-}$	Supply voltage, VS+ to VS–	7	V
V_{CM}	Common mode input voltage	V_{S-}– 0.3 to V_{S+} +0.3	V
ESD	Electrostatic discharge voltage	HBM ±4000	V
		CDM ±1000	V
T_J	Junction temperature	160	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{JL}	Soldering temperature range (soldering 10 seconds)	260	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. Input terminals are diode clamped to the supply rails.
3. The device is provided such that the maximum junction temperature (TJ) will not be exceeded at any time.

Electrical parameters (TA=25℃)

(VS=5.0V, TA=+25℃, VCM=VS/2, VO=VS/2, RL=10kΩ connect to VS/2, unless otherwise stated.)

Symbol	Parameter	condition	Min	Typ	Max	Unit
Input characteristics						
V_{OS}	Input offset voltage		-4.2	±0.8	4.2	mV
	Full temperature		-4.5		4.5	
$V_{OS}TC$	Offset voltage drift			2		μV/°C
I_B	Input bias current			1		
	Full temperature			800		pA
I_{OS}	Input offset current			1		pA
V_{CM}	Common mode voltage range		V_{S-}–0.1		V_{S+}+0.1	V
CMRR	Common mode rejection ratio	V_{CM}= 0.05V to 3.5V	66	84		dB
	Full temperature			80		
		V_{CM}= V_{S-}–0.1 to V_{S+}+0.1V	60	76		
A_{VOL}	Open loop voltage gain	R_L =10kΩ, V_O = 0.05 to 3.5V	90	103		
	Full temperature			90		
		R_L = 600Ω, V_O =0.15 to 3.5V	77	86		
	Full temperature			80		
R_{IN}	Input resistance			100		GΩ
C_{IN}	Input capacitance	Differential mode		2		pF
		Common mode		3.5		
V_{OH}	High output voltage swing	R_L=600Ω		V_{S+}–130		mV
		R_L=10kΩ		V_{S+}–12		
V_{OL}	Low output voltage swing	R_L=600Ω		120		mV
		R_L=10kΩ		7		
Z_{OUT}	Closed loop output impedance	f= 200kHz,G = +1		0.4		Ω
	Open loop output impedance	f=1MHz, I_O=0		2.6		
I_{SC}	Short circuit current	Sink current		40		mA
		Source current		40		

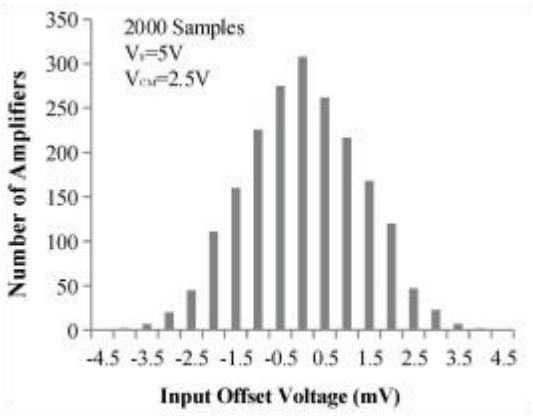
Electrical parameters (TA=25℃)

(VS=5.0V, TA=+25°C, VCM=VS/2, VO=VS/2, RL=10kΩ connect to VS/2, unless otherwise stated.)

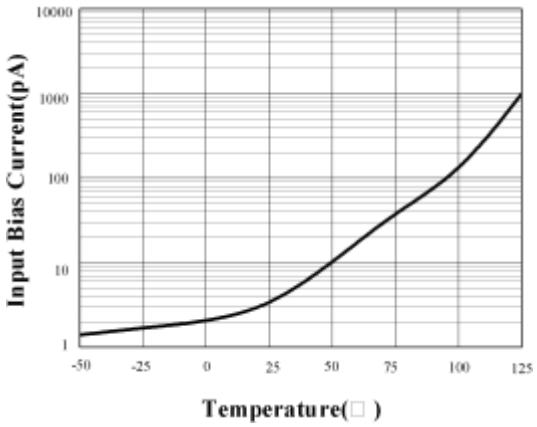
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Dynamic performance						
GBW	Gain bandwidth product			6.5		MHz
Φ_M	Phase margin	C_L=100pF		60		°
SR	Slew rate	G = +1,C_L =100pF,V_O=1.5V to 3.5V		4		V/μs
BW_P	Full power bandwidth	<1% distortion		300		kHz
t_S	Build time	0.1%, G = +1（2V step）		1		
		0.01%, G = +1（2V step）		1.2		μs
t_{OR}	Overload recovery time	V_{IN} ×Gain> V_S		0.5		μs
Noise performance						
V_n	Input voltage noise	f= 0.1 to 10Hz		12		μV_{P-P}
e_n	Input voltage noise density	f=10kHz		20		nV/√Hz
I_n	Input current noise density	f=10kHz		5		fA/√Hz
Power supply						
V_S	Supply voltage		2.1		5.5	V
PSRR	Power supply rejection ratio	V_S= 2.7V to 5.5V, V_{CM}< V_{S+}− 2V	70	84		dB
	Full temperature			80		
I_Q	Quiescent current (per amplifier)			480	560	μA
	Full temperature			520	620	
Thermal properties						
T_A	Temperature range		-40		125	°C
θ_{JA}	Package thermal impedance	SC70-5		333		°C/W
		SOT23-5		190		
		MSOP-8		216		
		SO-8		125		
		DFN-8L		201		
		TSSOP-8		153		
		TSSOP-14		112		
		SO-14		115		

Typical performance characteristics

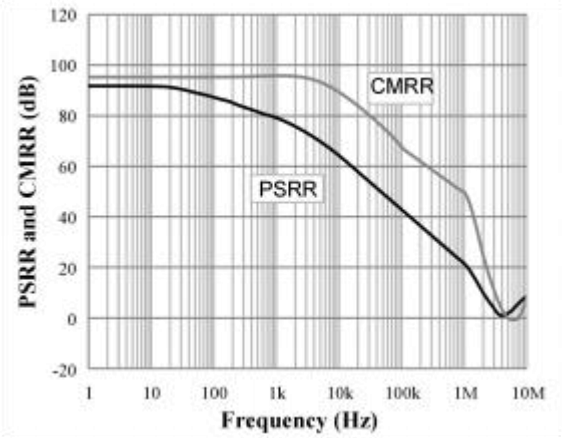
(T_A=+25℃, V_{CM}=V_S/2, R_L=10kΩ connect to V_S/2, unless otherwise stated.)



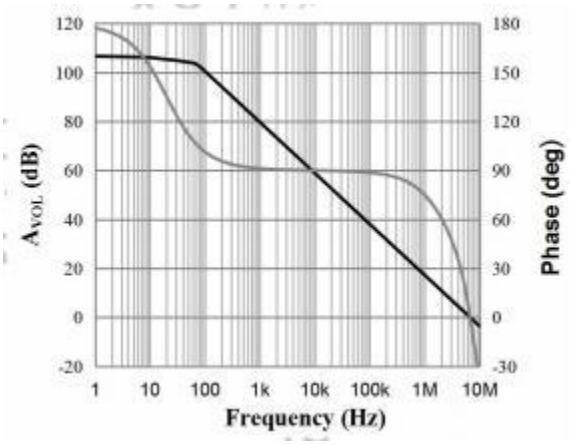
Picture 2. Input offset voltage distribution



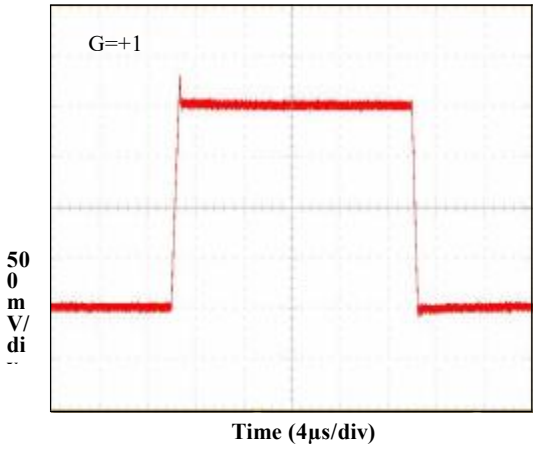
Picture 3. Input bias current vs. temperature



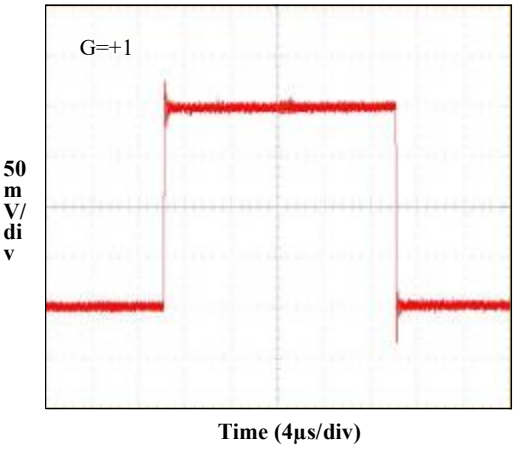
Picture 4. Power supply rejection ratio and common mode rejection ratio vs. frequency



Picture 5. Open-loop gain and phase margin vs. frequency



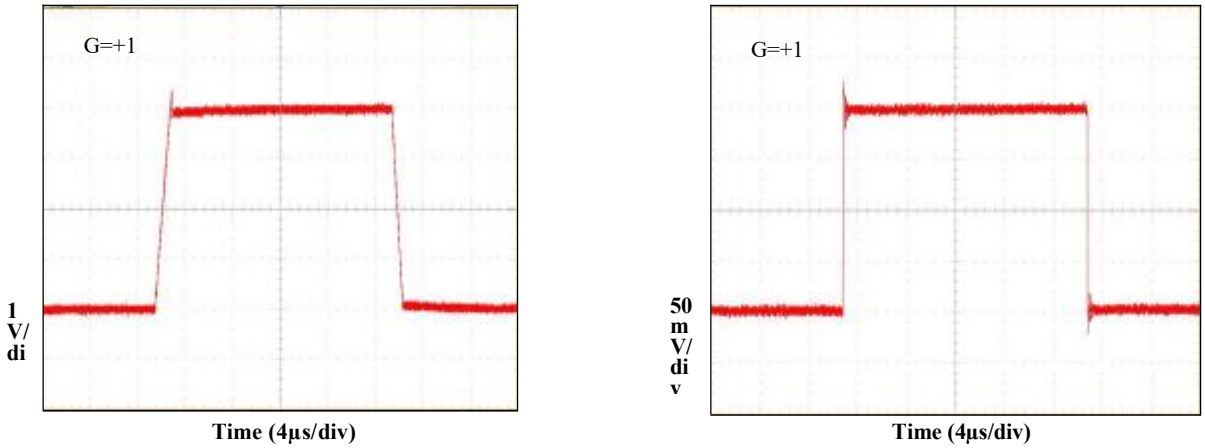
Picture 6. Large signal step response at 2.7V



Picture 7. Small signal step response at 2.7V

Typical performance characteristics

(T_A=+25℃, V_{CM}=V_S/2， R_L=10kΩ connect to V_S/2, unless otherwise stated.)



Picture 8. Large signal step response at 5V Small signal step response at 5V

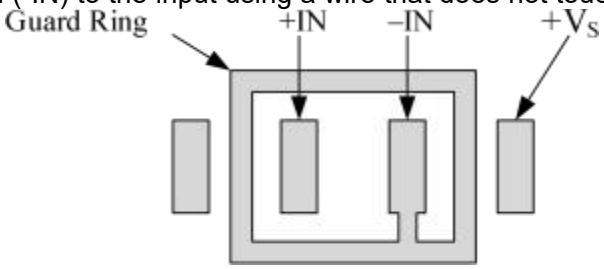
Application notes

1.Low input bias current

The SL863x is a family of CMOS operational amplifiers that feature very low input bias currents in the pA range. The low input bias current allows the amplifier to be used in applications with high resistance sources, but care must be taken to minimize PCB surface leakage. See the PCB surface leakage section below for more information.

2.PCB surface leakage

In applications where input bias current requirements are low, the effects of printed circuit board (PCB) surface leakage need to be considered. Surface leakage is caused by moisture, dust, or other contaminants on the board. Under low humidity conditions, the typical resistance between adjacent traces is 1012Ω, and a voltage difference of 5V between the two causes a current of 5pA to flow, which is greater than the input bias current of the SL863x at +25°C (typical value ±1pA). It is recommended to use a multilayer PCB layout and route the op amp's –IN and +IN signals below the PCB surface.
An effective way to reduce surface leakage is to use a guard ring around the sensitive pin (or trace). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 10 for an inverting gain application.
1. For non-inverting gain and unity gain buffers:
a) Connect the non-inverting pin (+IN) to the input using a wire that does not touch the PCB surface.
b) Connect the guard ring to the inverting input pin (-IN). This biases the guard ring to the common-mode input voltage.
2. For inverting gain and transimpedance gain amplifiers (converting current to voltage, such as photodetectors):
a) Connect the guard ring to the noninverting input pin (+IN). This biases the guard ring to the same reference voltage as the op amp (for example, VS/2 or ground).
b) Connect the inverting pin (-IN) to the input using a wire that does not touch the PCB surface.

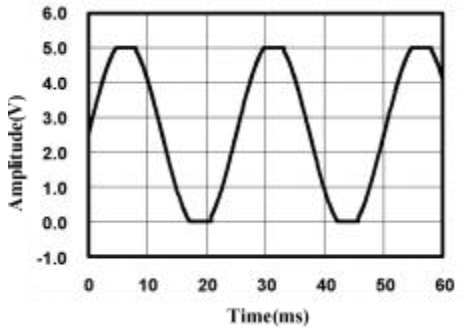


Picture 10. Use guard rings around sensitive pins

Application notes

3.Rail-to-Rail Features

The input common-mode voltage range of the SL863x family can extend 300mV beyond the supply rails. This is achieved with a complementary input stage—an N-type MOS input differential pair in parallel with a P-type MOS input differential pair. For normal operation, the inputs should be limited to this range. The absolute maximum input voltage is 500mV beyond the supplies, and inputs greater than the input common-mode range but less than the maximum input voltage are invalid but will not cause any damage to the op amp. Unlike some other op amps, the inputs can extend beyond the supplies without phase flipping if the input current is limited, as shown in Figure 11. Since the input common-mode range extends from (VS−− 0.1V) to (VS++ 0.1V), the SL863x op amps can achieve “true ground” sensing.



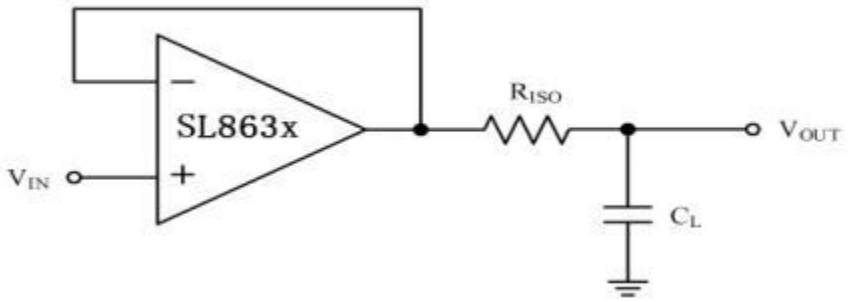
Picture 11. No phase reversal when input exceeds supply voltage

The class AB output stage topology with common-source transistors allows rail-to-rail output. For light resistive loads (e.g. 100kΩ), the output voltage can typically swing to within 5mV of the rails. With moderate resistive loads (e.g. 10kΩ), the output can typically swing to within 15mV of the rails and maintain high open-loop gain.
The maximum output current is related to the total supply voltage. As the supply voltage of the amplifier increases, the output current capability also increases. Care must be taken to keep the junction temperature of the IC below 150°C when the output is continuously shorted. The outputs of the amplifier have reverse-biased ESD diodes connected to each supply. The output should not be forced to exceed 0.5V of either supply, otherwise current will flow through these diodes.

4.Capacitive soading and stability

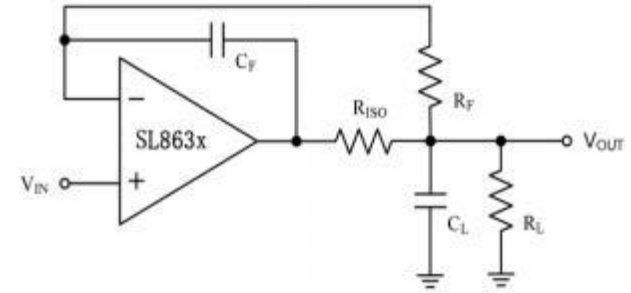
The SL863x can drive 1nF directly at unity gain without oscillation. Unity-gain followers (buffers) are the most sensitive circuits to capacitive loads.
Driving capacitive loads directly degrades the amplifier’s phase margin, causing ringing or even oscillation. Applications that require greater capacitive drive capability should use an isolation resistor between the output and the capacitive load, as in the circuit in Figure 12. The isolation resistor, R_{ISO}, and the load capacitor, C_L, form a zero to improve stability. The larger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this approach results in a loss in gain accuracy because R_{ISO} forms a voltage divider with R_L.

Application notes



Picture 12. Indirectly drives heavy capacitive loads

The improved circuit is shown in Figure 13. It provides DC accuracy while ensuring AC stability. R_F provides DC accuracy by connecting the inverted signal to the output.
C_F and R_{ISO} offset the loss of phase margin by feeding the high frequency component of the output signal back to the inverting input of the amplifier, thereby maintaining phase margin throughout the feedback loop.



Picture 13. Indirectly drives heavy capacitive loads with DC precision

For circuits with non-unity gain, there are two other ways to increase phase margin: (a) by increasing the gain of the amplifier, or (b) by adding a capacitor in parallel with the feedback resistor to cancel the parasitic capacitance associated with the inverting node.

5.Power supply layout and filtering

The SL863x family operates from a single +2.1V to +5.5V supply or a dual ±1.05V to ±2.25V supply. For single-supply operation, filter ceramic capacitors (0.01μF to 0.1μF) should be placed close to the VS pin (within 2mm for good high-frequency performance). For dual-supply operation, the VS+ and VS– supplies should be connected to ground through separate 0.1μF ceramic capacitors. Bulk capacitors (2.2μF or larger tantalum capacitors) within 100mm provide large, slow currents and better performance. The bulk capacitors can be shared with other analog devices. Good PCB layout techniques optimize performance by reducing stray capacitance at the op amp input and output. To reduce stray capacitance, minimize trace length and width by placing external devices as close to the chip as possible, and use surface mount devices whenever possible. For op amps, it is strongly recommended to solder the device directly to the PCB board and keep the high-frequency, high-current loop area as small as possible to reduce EMI (electromagnetic interference).

Application notes

6.Ground

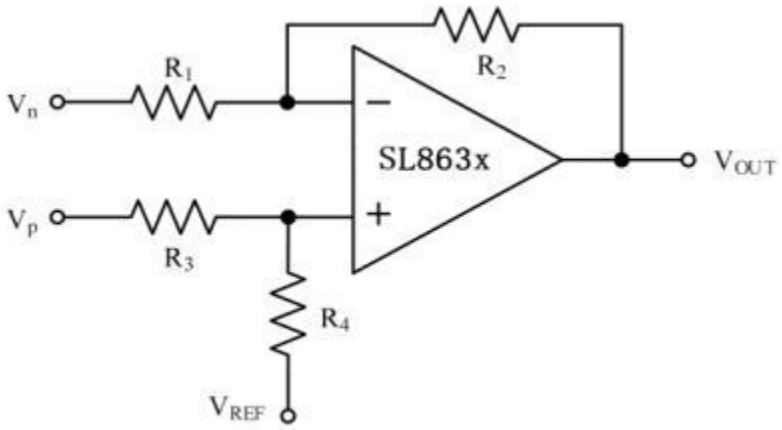
In SL863x circuit design, the ground plane is very important. The length of the current path in the inductive ground return line will generate unwanted voltage noise, and a wide ground area will reduce parasitic inductance.

7.Input and output coupling

To minimize capacitive coupling, input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

Typical application circuit diagram

1.Differential amplifier

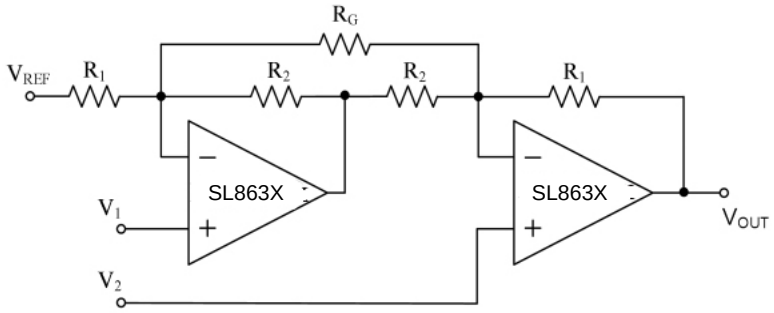


Picture 14. Differential amplifier

The circuit shown in Figure 14 implements the differential function. If the resistor ratio is equal to R4/R3 = R2/R1, then：

$$V_{OUT}= (V_p- V_n)\times R_2/R_1 + V_{REF}$$

2.Instrumentation amplifier



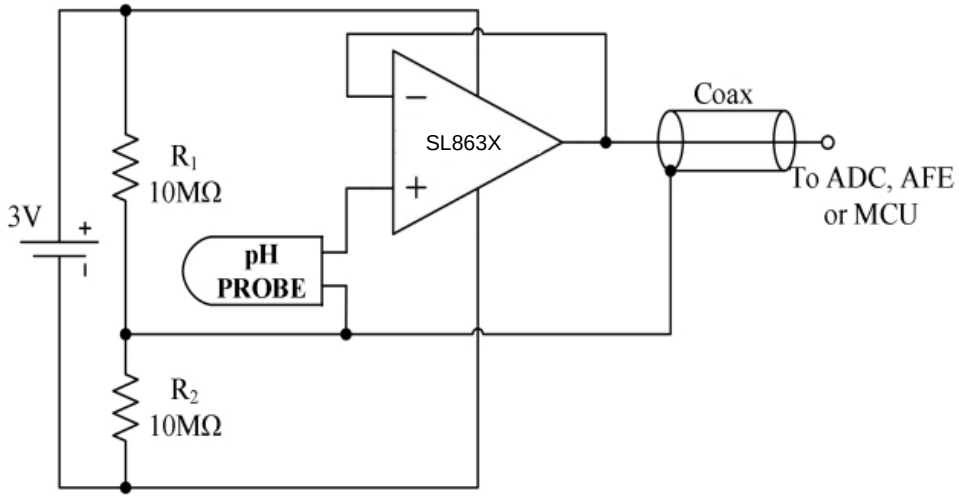
$$V_{OUT}=(V_1-V_2)(1+\frac{R_1}{R_2}+\frac{2R_1}{R_G})+V_{REF}$$

Picture 15. Instrumentation amplifier

The SL863x family is well suited for conducting sensor signals in battery-powered applications. Figure 15 shows an instrumentation amplifier using two op amps from the SL863x family. This circuit is useful in applications where common-mode noise rejection with higher gain is required. The reference voltage (V_{REF}) is provided by a low impedance source, and in single-supply voltage applications, V_{REF} is typically VS/2.

Typical application circuit diagram

3.Chemical Sensors



Picture 16. pH probes

The input bias current of the SL863x family is in the pA range. This is ideal for buffering high impedance chemical sensors such as pH probes. For example, the circuit in Figure 16 eliminates the bulky low leakage cables required to connect a pH probe (common combination pH probes such as the Corning 476540) to a metering IC such as an ADC, AFE, and/or MCU. An SL863x op amp and a lithium battery are installed in the probe assembly. A conventional low-cost coaxial cable can be used to transmit the output signal of the op amp to a subsequent IC to read the pH value.

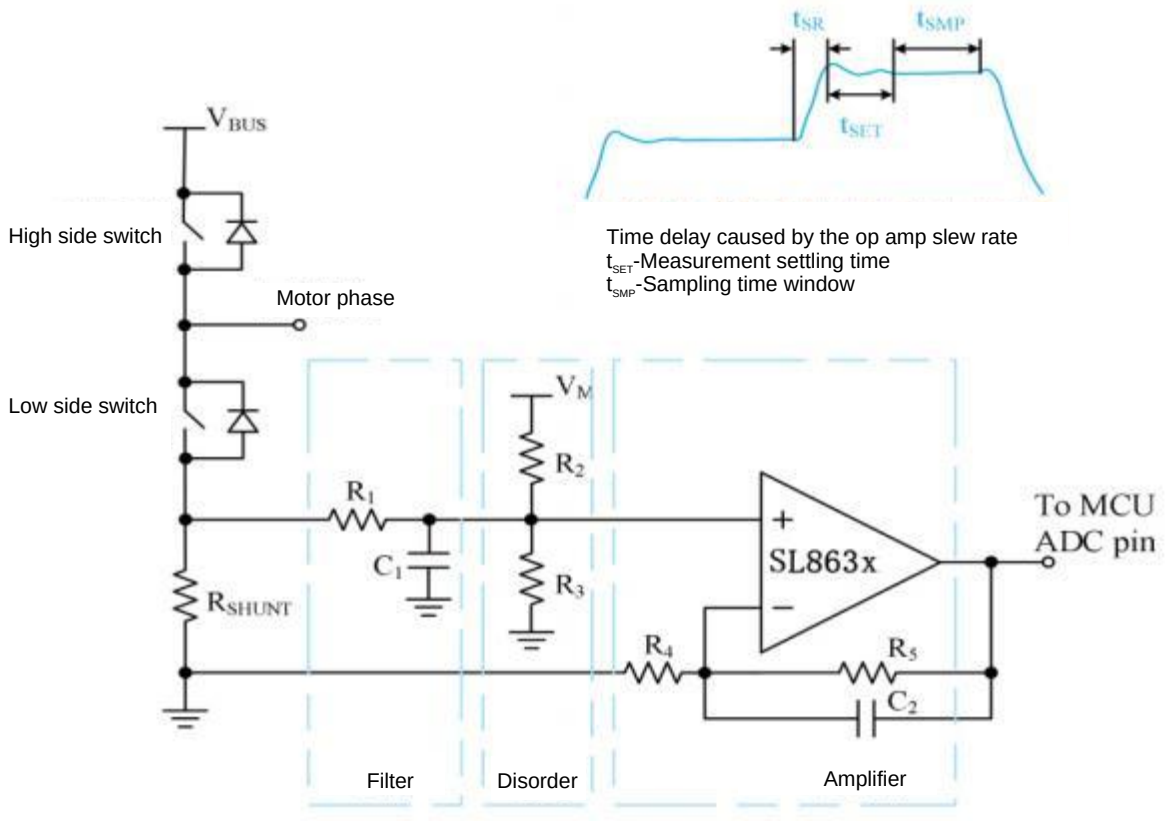
4. Shunt-based current sense amplifier

The current sense amplifier shown in Figure 17 has a slew rate of 2πfVPP for the output sine wave signal and a slew rate of 2fVPP for the output triangle wave signal. In most motor control systems, the PWM frequency is between 10kHz and 20kHz. For a PWM frequency of 10kHz, one cycle time is 100μs. In the shunt monitoring of the motor, the phase current is converted into a phase voltage signal for ADC sampling. The sampled voltage signal must be settled before entering the ADC. As shown in Figure 8, the total settling time of the current shunt monitor circuit includes the rising edge delay time (tSR) caused by the slew rate of the operational amplifier, and the measurement settling time (tSET). If the minimum duty cycle of the PWM is defined as 5%, and tSR is required for phase current monitoring at 20% of the total time window, then for a 3.3V motor control system (ADC with a 12-bit 3.3V MCU), the slew rate of the operational amplifier should be greater than:

$$3.3V/（100\mu s\times 5\%\times 20\%）=3.3V/\mu s$$

Also, the bandwidth of the op amp should be much larger than the PWM frequency (at least 10 times larger).

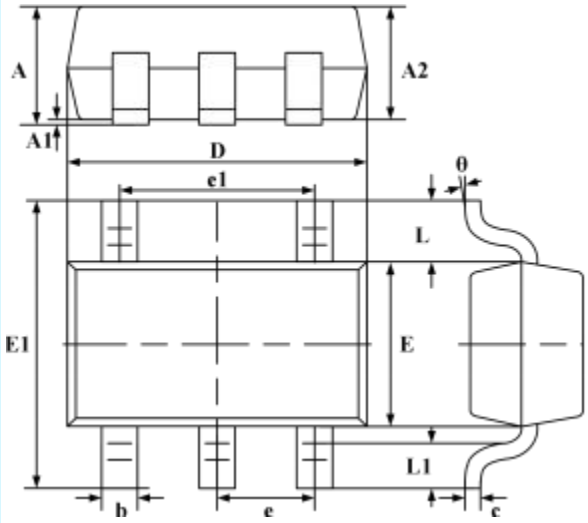
Typical application circuit diagram



Picture 17. Current shunt monitoring circuit

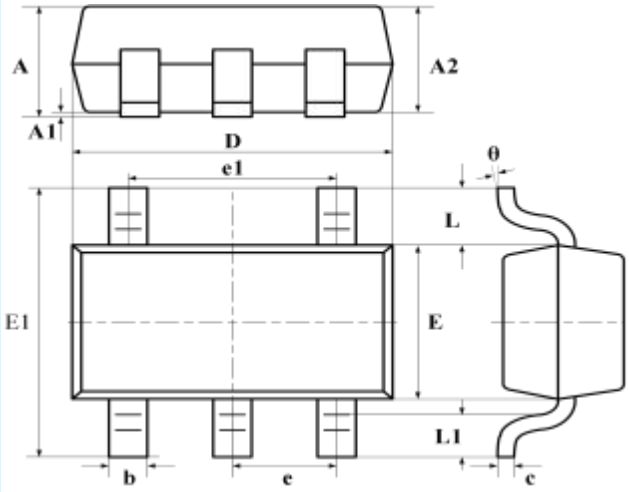
Package information

SC70-5 (SOT353)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	0.900	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.150	0.003	0.006
D	1.850	2.150	0.079	0.087
E	1.100	1.400	0.045	0.053
E1	1.950	2.200	0.085	0.096
e	0.850 typ.		0.026 typ.	
e1	1.200	1.400	0.047	0.055
L	0.42 ref.		0.021 ref.	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

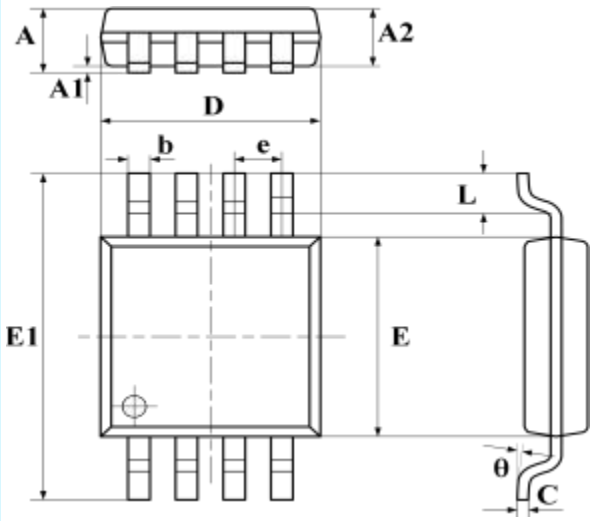
SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.040	1.350	0.042	0.055
A1	0.040	0.150	0.002	0.006
A2	1.000	1.200	0.041	0.049
b	0.380	0.480	0.015	0.020
c	0.110	0.210	0.004	0.009
D	2.720	3.120	0.111	0.127
E	1.400	1.800	0.057	0.073
E1	2.600	3.000	0.106	0.122
e	0.950 typ.		0.037 typ.	
e1	1.900 typ.		0.078 typ.	
L	0.700 ref.		0.028 ref.	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

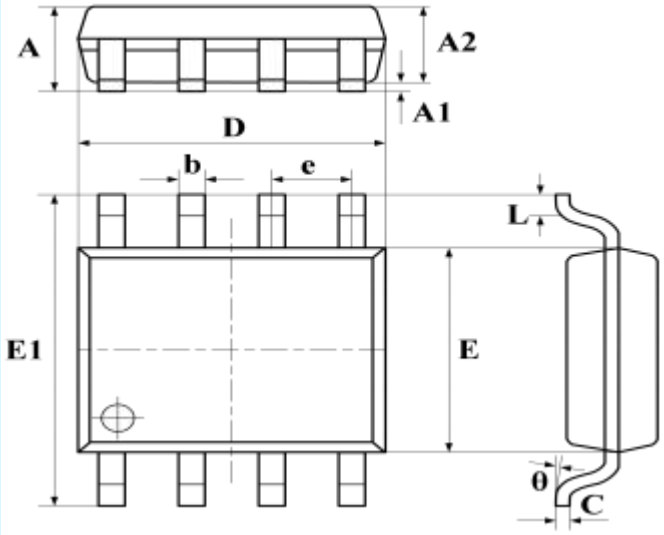
Package information

MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.033	0.045
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.031	0.039
b	0.290	0.380	0.012	0.016
C	0.150	0.200	0.006	0.008
D	2.900	3.100	0.118	0.127
E	2.900	3.100	0.118	0.127
E1	4.700	5.100	0.192	0.208
e	0.650 typ.		0.026 typ.	
L	0.400	0.700	0.016	0.029
θ	0°	8°	0°	8°

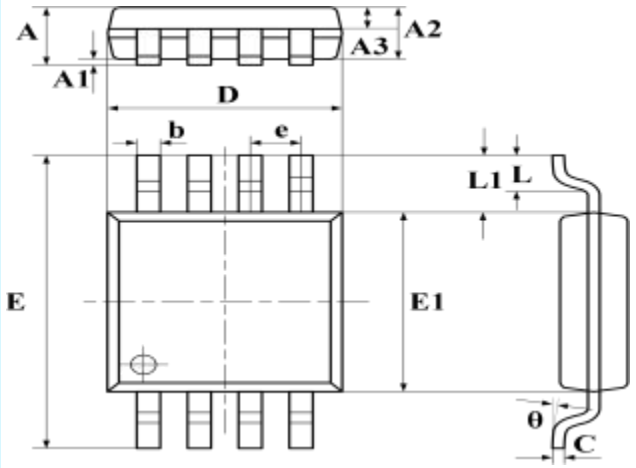
SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.370	1.670	0.056	0.068
A1	0.070	0.170	0.003	0.007
A2	1.300	1.500	0.053	0.061
b	0.306	0.506	0.013	0.021
C	0.203 typ.		0.008 typ.	
D	4.700	5.100	0.192	0.208
E	3.820	4.020	0.156	0.164
E1	5.800	6.200	0.237	0.253
e	1.270 typ.		0.050 typ.	
L	0.450	0.750	0.018	0.306
θ	0°	8°	0°	8°

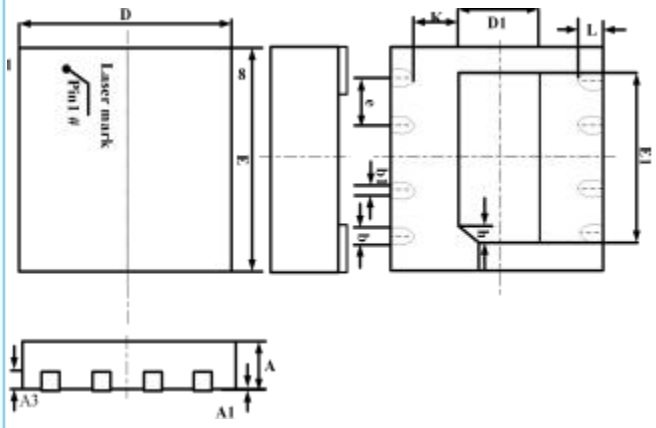
Package information

TSSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches
	Min	Nom	Max
A	-	-	1.200
A1	0.050	-	0.150
A2	0.900	1.000	1.050
A3	0.390	0.440	0.490
b	0.200	-	0.280
C	0.130	-	0.170
D	2.900	3.000	3.100
E	6.200	6.400	6.600
E1	4.300	4.400	4.500
e	0.65BSC		
L	0.450	-	0.750
L1	1.000 ref		
θ	0°	-	8°

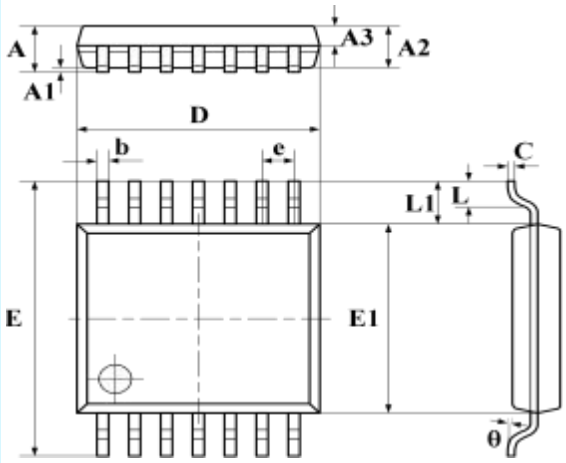
DFN8-L 2*2



Symbol	Dimensions In Millimeters		
	Min	Nom	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	0.203REF		
b	0.200	0.2500	0.300
b1	0.180REF		
D	1.900	2.000	2.100
E	1.900	2.000	2.100
e	0.500BSC		
D1	0.500	0.600	0.700
E1	1.100	1.200	1.300
L	0.300	0.350	0.40
K	0.35REF		
h	0.200REF		

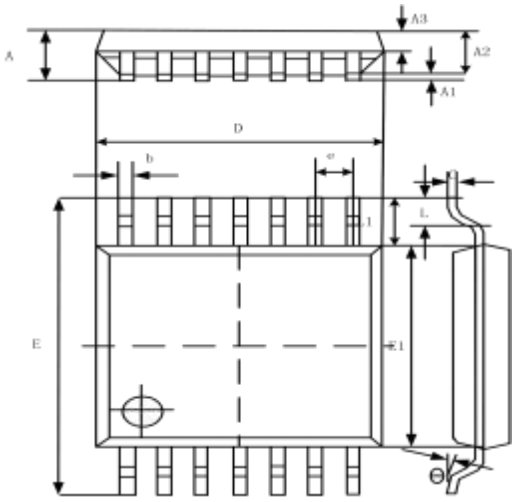
Package information

TSSOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.200	-	0.0472
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.037	0.043
A3	0.390	0.490	0.016	0.020
b	0.200	0.290	0.008	0.012
C	0.130	0.180	0.005	0.007
D	4.860	5.060	0.198	0.207
E	6.200	6.600	0.253	0.269
E1	4.300	4.500	0.176	0.184
e	0.650 typ.		0.0256 typ.	
L1	1.000 ref.		0.0393 ref.	
L	0.450	0.750	0.018	0.031
θ	0°	8°	0°	8°

SOP-14



Symbol	DimensionsI n Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.450	1.850	0.059	0.076
A1	0.100	0.300	0.004	0.012
A2	1.350	1.550	0.055	0.063
A3	0.550	0.750	0.022	0.031
b	0.406typ.		0.017typ.	
C	0.203typ.		0.008typ.	
D	8.630	8.830	0.352	0.360
E	5.840	6.240	0.238	0.255
E1	3.850	4.050	0.157	0.165
e	1.270 typ.		0.050 typ.	
L1	1.040 ref.		0.041 ref.	
L	0.350	0.750	0.014	0.031
θ	2°	8°	2°	8°